In the Claims:

1. (Currently Amended) A CMOS structure having a stress creating contact etch stop silicon nitride layer ~~in which stress is relaxed by implantation therein of~~ including oxygen-containing or carbon-containing ions.

2. (Currently Amended) The structure of Claim 1 in which ~~stress is relaxed in a selected area by preventing ion implantation in all but the selected area~~ regions of the silicon nitride layer are free from the oxygen-containing or carbon-containing ions.

3. (Canceled)

4. (Original) The structure of Claim 1 in which the stress in the layer is tensile.

5. (Currently Amended) The structure of Claim 4, which further comprises a PMOS device and an NMOS device both covered by the layer, and wherein ~~implantation of oxygen-containing or carbon-containing ions is prevented~~ there are no oxygen-containing or carbon-containing ions in the area of the silicon nitride layer overlying the NMOS device.

6. (Original) The structure of Claim 1 in which the stress in the layer is compressive.

7. (Currently Amended) The structure of Claim 6, which further comprises a PMOS device and an NMOS device both covered by the silicon nitride layer, and wherein ~~implantation of the oxygen-containing or carbon-containing ions is prevented~~ there are no oxygen-containing or carbon-containing ions in the area of the layer overlying the PMOS device.

8. (Original) A CMOS structure having a silicon nitride contact etch stop layer overlying one or more NMOS devices and one or more PMOS devices, comprising:

first areas of the layer overlying one type of device and having oxygen-containing or carbon-containing ions implanted therein; and

second areas of the layer overlying the other type of device and not having oxygen-containing or carbon-containing ions implanted therein.

9. (Original) The structure of Claim 8, wherein the layer is formed by chemical vapor deposition.

10. (Original) The structure of Claim 8, wherein the layer is formed by thermal chemical vapor deposition.

11. (Original) The structure of Claim 10, wherein:

the first areas overlie the PMOS devices; and

the second areas overlie the NMOS devices.

12. (Original) The structure of Claim 8, wherein the layer is formed by plasma enhanced chemical vapor deposition.

13. (Original) The structure of Claim 12, wherein:

the first areas overlie the NMOS devices; and

the second areas overlie the PMOS devices.

14. (Original) A method of relaxing stress in a silicon nitride layer of a CMOS structure comprising implanting oxygen-containing or carbon-containing ions into the layer.

15. (Original) The method of Claim 14, further comprising preventing oxygen-containing or carbon-containing ion implantation in all but the selected area of the layer.

16. (Original) The method of Claim 15, wherein the preventing step is effected by masking all but the selected area of the layer.

17. (Original) The method of Claim 14, wherein the stress in the layer is tensile.

18. (Original) The method of Claim 17, wherein the layer is superjacent to a PMOS device and to an NMOS device, and further comprising preventing oxygen-containing or carbon-containing ion implantation into the area of the layer overlying the NMOS device.

19. (Original) The method of Claim 18, wherein the preventing step is effected by masking all but the area of the layer overlying the PMOS device.

20. (Original) The method of Claim 19, wherein the masking step is effected by selectively applying and developing a photoresist coating on the layer.

21. (Original) The method of Claim 14, wherein the stress in the layer is compressive.

22. (Original) The method of Claim 21, wherein the layer is superjacent to a PMOS device and to an NMOS device, and further comprising preventing oxygen-containing or carbon-containing ion implantation into the area of the layer overlying the PMOS device.

23. (Original) The method of Claim 22, wherein the preventing step is effected by masking all but the area of the layer overlying the NMOS device.

24. (Original) The method of Claim 23, wherein the masking step is effected by selectively applying and developing a photoresist coating on the layer.

25. (Original) A method of relaxing the stress in a silicon nitride contact etch stop layer overlying one or more NMOS devices and one or more PMOS devices, comprising:

selectively implanting oxygen-containing or carbon-containing ions into areas of the layer overlying one type of device; and

simultaneously preventing implantation of the ions into areas of the layer overlying the other type of device.

26. (Original) The method of Claim 25, wherein the preventing step is effected by masking the areas of the layer overlying the other type of device.

27. (Original) The method of Claim 26, wherein the masking step is effected by selectively applying and developing a photoresist coating on the layer.

28. (Original) The method of Claim 25, wherein the layer is formed by chemical vapor deposition.

29. (Original) The method of Claim 25, wherein the layer is formed by thermal chemical vapor deposition.

30. (Original) The method of Claim 29, wherein the developed photoresist masks the NMOS devices.

31. (Original) The method of Claim 25, wherein the layer is formed by plasma enhanced chemical vapor deposition.

32. (Original) The method of Claim 31, wherein the developed photoresist masks the PMOS devices.